REMARKS

In the Drawings

Drawing Objections under U.S.C. § 1.84(p)(5)

The drawings were objected to under 37 U.S.C. § 1.84(p)(5), as having a reference sign (command register 133 in Figure 1A) that is not mentioned in the description; and for not including a reference sign mentioned in the description (address inputs 133 of page 8, line 11).

Applicant notes that the address inputs 133 are labeled in Figure 1A as described in the description at page 8, line 11, but that this is duplicate with the reference sign of the command register 133. Applicant has enclosed a red-line copy of Figure 1A re-labeling the command register from 133 to 135 to correct this typographical error.

Applicant has also amended the specification to describe the command execution logic 130 as containing a command register 135. Applicant submits that this amendment does not constitute new matter because the command register element is in the command execution logic 130 in the original Figure 1A. Applicant respectfully requests approval of the changes to Figure 1A and the supporting amendments to the specification. Applicant will submit revised formal drawings to the Draftsperson upon approval by the Examiner.

The Applicant respectfully submits that the proposed changes to Figure 1A and the description do not comprise new matter and that the requirements of 37 U.S.C. § 1.84(p)(5) are satisfied. Applicant therefore requests that the objection under 37 U.S.C. § 1.84(p)(5) be withdrawn.

In the Specification

The disclosure was objected to because of informalities: The abbreviations PCS and BIOS not being explained in the description (page 1, line 30).

Applicant has amended the specification to explain the abbreviations. Applicant submits that this amendment would not constitute new matter because these abbreviations

are well known to those of ordinary skill in the art within the context in which they are used. Applicant therefore respectfully requests approval of the amendment to the specification and that the objection be withdrawn.

Claim Objections

Rejections Under 35 U.S.C. § 112

Claims 1-27 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The Examiner based the rejection upon the command register 133 of Figure 1A not being described. The Examiner further stated that the features as recited in claims 2, 19-20, and 22-23 were not described in the specification.

Applicant respectfully traverses the rejection. As stated above, Applicant has enclosed a proposed red-line copy of Figure 1A re-labeling the command register from 133 to 135 to correct a typographical error. Applicant has also amended the specification to describe the command execution logic 130 as containing a command register 135. Applicant submits that this amendment does not constitute new matter because the command register element is in the command execution logic 130 in the original Figure 1A. Furthermore, the command register element 135 is not essential to an understanding of the claimed subject matter.

The Applicant also respectfully submits, in addition to the above arguments, that the 35 U.S.C. § 112 rejection was inappropriately applied. Applicant maintains that claims 1-27 contain subject matter that was described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. The Applicant respectfully submits that the description or Figures of the Application having a feature that was not recited in claims 1-27 and not essential to the claims cannot support the § 112 rejection. The Applicant therefore requests that the rejection of claims 1-27 under 35 U.S.C. § 112, first paragraph, be withdrawn.

Applicant is also unsure as to which features of claims 2, 19-20, and 22-23 that the Examiner claimed were not described in the specification. Applicant contends that relevant features of claims 2, 19-20, and 22-23 have been described in the specification to allow one skilled in the art to practice the invention. Therefore Applicant requests that the rejection of claims 2, 19-20, and 22-23 under 35 U.S.C. § 112, first paragraph, be withdrawn.

Applicant respectfully requests that the rejection of the claims 1-27 be withdrawn in light of the above amendments and that the specification does clearly describe the invention in a way to enable one skilled in the art to make or use the invention.

Rejections Under 35 U.S.C. § 102

Claims 1-13 were rejected under 35 U.S.C. § 102 (b) as being anticipated by Cowles et al. (U.S. Patent 5,263,003).

Applicant respectfully traverses this rejection and requests reconsideration of the claims. Applicant feels that claims 1-13 are allowable for the following reasons.

The Examiner states that Figures 1-3 of Cowles et al. detail a synchronous flash memory system citing line 27 of column 5 of Cowles et al. The Examiner further stated that the write cycle immediately followed a read cycle, citing lines 40-62 of column 7.

Applicant respectfully maintains that lines 24-27 of column 5 describe only the serial I/O (SIO) 42 of Figure 2 and does not teach or disclose a synchronous flash memory system. Applicant therefore submits that the cited reference does not teach or describe a synchronous flash memory in the detailed description or drawings. Additionally, Applicant also respectfully maintains that Cowles et al. at lines 40-62 of column 7 describes a burst addressing mode of multiple consecutive reads or multiple consecutive writes and does not teach or disclose a write cycle immediately followed by a read cycle.

Applicant respectfully submits that Cowles et al. does not teach or disclose a method of writing to a synchronous non-volatile memory device by receiving write data

on a first clock cycle and executing a data write operation and executing a data read operation on a next clock cycle immediately following the first clock cycle.

Applicant also notes that Cowles et al. is directed to a memory controller and a flash memory system having multiple individual flash memory devices and not a synchronous non-volatile memory device.

Applicant respectfully contends that claims 1-13 have been shown to be patentably distinct from the cited reference. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(b) and allowance of claims 1-13.

Claims 14-27 were rejected under 35 U.S.C. § 102 (b) as being anticipated by Patel (U.S. Patent 5,539,696).

Applicant respectfully traverses this rejection and requests reconsideration of the claims. Applicant feels that claims 14-27 are allowable for the following reasons.

The Examiner states that Figure 1 details a synchronous memory system 10 which can be used with nonvolatile EEPROM, PROM, or ROM devices citing lines 22-25 of column 4 of Patel. The Examiner also stated that synchronous memory cell array 14 is coupled to the input/output data buffer circuit I/O 26 of Figure 1. The Examiner further stated the synchronous memory included write latches 102, 104, 106, 108, and 110 as shown in Figure 3.

Applicant respectfully maintains that Figure 1 of Patel teaches a separate synchronous peripheral I/O device 26 coupled to a digital processor 12 and a synchronous DRAM device 14 and not does not teach or disclose a system having a synchronous non-volatile memory wherein the synchronous memory has an input/output data buffer. *See, e.g.,* Patel, column 4, lines 31-37. Applicant also maintains that Figure 3 of Patel teaches an input buffer 100 that contains latches 102, 104, 106, and 108 and a write latch control circuit 110 and does not teach or disclose a data buffer coupled to a write latch. *See, e.g.,* Patel, column 11, lines 31-38.

Applicant therefore respectfully submits that Patel does not teach or disclose a memory system having a processor and a synchronous memory device coupled to the processor via a bi-directional data bus. The synchronous memory device comprising a memory array arranged in rows and columns, data communication connections coupled to the bi-directional data bus, an input/output data buffer coupled to the data communication connections to manage bi-directional data communication, and a write latch coupled between the data buffer and the memory array to latch data provided on the data communication connections.

Applicant also notes that Patel mentions but does not teach or disclose a synchronous memory system that is utilized with EEPROM, PROM, or ROM devices. Applicant respectfully submits that mentioning EEPROM, PROM, or ROM devices would not enable one skilled in the art to practice the disclosed invention of Patel with synchronous non-volatile memory devices.

Applicant respectfully contends that claims 14-27 have been shown to be patentably distinct from the cited reference. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(b) and allowance of claims 14-27.

CONCLUSION

In view of the above remarks, Applicant respectfully submits that the claims are in condition for allowance and requests reconsideration of the application and allowance of claims.

The Examiner is invited to contact Applicant's Representatives at direct dial (612) 312-2207 if there are any questions regarding this Response or if prosecution of this application may be assisted thereby.

Respectfully submitted,

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Andrew C. Walseth
Reg. No. 43,234

Attorneys for Applicant
Leffert Jay & Polglaze, P.A.
P.O. Box 581009
Minneapolis, MN 55458-1009
telephone: (612) 312-2200
facsimile: (612) 312-2250

MARKED-UP VERSION

IN THE SPECIFICATION

Please replace the paragraph starting on page 1, line 28 with the following amended paragraph:

Yet another type of non-volatile memory is a Flash memory. A Flash memory is a type of EEPROM that can be erased and reprogrammed in blocks instead of one byte at a time. Many modern personal computers (PCS) have their basic input/output system (BIOS) stored on a flash memory chip so that it can easily be updated if necessary. Such a BIOS is sometimes called a flash BIOS. Flash memory is also popular in modems because it enables the modem manufacturer to support new protocols as they become standardized.

Please replace the paragraph starting on page 6, line 14 with the following amended paragraph:

Referring to Figure 1A, a block diagram of one embodiment of the present invention is described. The memory device 100 includes an array of non-volatile flash memory cells 102. The array is arranged in a plurality of addressable banks. In one embodiment, the memory contains four memory banks 104, 106, 108 and 110. Each memory bank contains addressable sectors of memory cells. The data stored in the memory can be accessed using externally provided location addresses received by address register 112. The addresses are decoded using row address multiplexer circuitry 114. The addresses are also decoded using bank control logic 116 and row address latch and decode circuitry 118. To access an appropriate column of the memory, column address counter and latch circuitry 120 couples the received addresses to column decode circuitry 122. Circuit 124 provides input/output gating, data mask logic, read data latch circuitry and write driver circuitry. Data is input through data input registers 126 and

output through data output registers 128. Command execution logic 130, having a command register 135, is provided to control the basic operations of the memory device. A state machine 132 is also provided to control specific operations performed on the memory arrays and cells. A status register 134 and an identification register 136 can also be provided to output data.